PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
S2040 GC/sta		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP 02/11366	10.10.2002	10.10.2002
International Patent Classification (IPC) or both national classification and IPC		
H04L7/033		
Applicant		
INFINEON TECHNOLOGIES AG et al		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☐ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
04.05.2004	04.11.2004
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INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/EP 02/11366

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-12	as originally filed

Claims, Numbers

4-10, 13-16	as originally filed
2, 3	received on 02.09.2004 with letter of 01.09.2004
1, 11	received on 23.10.2004 with letter of 22.10.2004

Drawings, Sheets

1/3-3/3	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:
   - ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

   ☒ the entire international application,

   ☐ claims Nos.

   because:

   ☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (specify):

   ☒ the description, claims or drawings *(indicate particular elements below)* or said claims Nos. are so unclear that no meaningful opinion could be formed *(specify)*:

   see separate sheet

   ☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

   ☐ no international search report has been established for the said claims Nos.

2. A meaningful international preliminary examination cannot be carried out due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

   ☐ the written form has not been furnished or does not comply with the Standard.

   ☐ the computer readable form has not been furnished or does not comply with the Standard.

Re Item III

Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

Insufficient Disclosure (Art. 5 PCT)

1. According to independent claims 1 and 11, two separate loops are formed, namely:

   - The first output of the first clock generator is connected to a first input of the first phase detector, and the first phase detector detects a difference between a rising edge of the data signal and a rising edge of a rising edges clock signal

   - The second output of the second clock generator is connected to a second input of the second phase detector, and the second phase detector detects a difference between a falling edge of the data signal and a falling edge of a falling edges clock signal

   Furthermore, according to claims 1 and 11, these two independently operating phase locked loops operate in a way that the detected phase difference is minimal. A person skilled in the art of phase locked loop theory, would configure these two loops to produce a respective clock signal such that the phase difference becomes zero in a steady or locked state.

   Furthermore, according to claims 1 and 11, a third clock generator then generates an extracted clock signal based on the average of the first phase difference and the second phase difference in a way that the probability distribution functions of the rising edges and falling edges of the data signal are individually averaged.

   Interpreting the average of a phase difference in a phase locked loop, for example, in the sense of an arithmetic mean, the corresponding feature may be interpreted in at least two different ways:

   - The arithmetic mean of a sequence of discrete samples of the first phase difference and the arithmetic mean of a sequence of discrete samples of the second phase difference are computed (i.e. averaging the differences separately). In this case both averages are zero, and it is consequently not

possible to produce a meaningful clock signal based on these averages.

- The arithmetic mean of one discrete sample of the first phase difference and one discrete sample of the second phase difference is computed. If the transitions in the first loop are subject to a random jitter, then the detected first phase difference will be a random signal with zero mean (as indicated with the probability density function (308) in Figure 3). Likewise, the detected second phase difference will be a random signal with zero mean. How to generate a clock signal based on two random signals which are devoid of any information remains entirely unclear.

To fill the teaching lacking in the claims with respect to the generation of the extracted clock signal, a person skilled in the art would consult to this end the description and the Figures. The description discloses in that respect on page 5 that the basic idea of the invention is to individually average the probability distribution functions of the rising and falling edges of the data signal using two independent phase locked loops. However, nothing is disclosed in the description which would render it apparent to the skilled person how to compute these probability distribution functions based on the phase averages (which are either zero, or a random signal with zero mean, as outlined above). Furthermore, the description is completely silent about how the generation of the extracted clock signal results in the individual averaging of the probability distribution function. It is also pointed out that it is entirely unclear what the average of a probability distribution function might be, since it is an average in itself. Therefore, the description does not disclose the invention's essential features in sufficient detail to render it apparent to the skilled person how to put the invention into practice. The Figures do not disclose any additional information with respect to the generation of the extracted clock signal, either.

To the argument that the phase difference of the phase locked loops in a transient or out-of-lock state may be useful in order to generate the extracted clock signal, it is noted that nothing to that respect is mentioned in the description about this very complicated matter. To the person skilled in the art, it is by no means apparent how any useful information may be extracted from a transient state or an out-of-lock state of a PLL.

The only other information provided by the description with respect to the generation of the extracted clock signal is that, in a further embodiment, the

controller controls the generation of said clock signal so that the error rate of the extracted data is minimized (see, for example, the description on page 7, lines 5-8 or page 11, lines 1-2). This embodiment, however, also lacks the disclosure of precise technical features which would render it apparent to the skilled person how to generate the extracted clock signal.

2. Since neither the description nor the Figures disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art, they are considered so unclear that no meaningful opinion can be formed on the novelty, inventive step, or industrial applicability of the claimed invention (Articles 5 and 34(4)(a)(ii) PCT).

New Claims:

1. A clock signal extraction device for extracting an extracted clock signal out of a periodic data signal, comprising:

- a first clock generator (110) for generating the rising edges clock signal and a first phase detector (104) for detecting a first phase difference between a rising edge of the periodic data signal and a rising edge of the rising edges clock signal, the first clock generator (110) comprising a first output connected to a first input of the first phase detector (104) forming a first loop, the first clock generator (110) and the first phase detector (104) are coupled via the first loop and operate in a way that the detected first phase difference is minimal,
- a second clock generator (112) for generating the falling edges clock signal and a second phase detector (106) for detecting a second phase difference between a falling edge of the data signal and a falling edge of the falling edges clock signal, the second clock generator (112) comprising a second output connected to a second input of the second phase detector 106 forming a second loop, the second clock generator (112) and the second phase detector (106) are coupled via the second loop and operate in a way that the detected second phase difference is minimal,
- a third clock generator (114) for generating the extracted clock signal based on an average of the first phase difference and the second phase difference in a way that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged.

11. A method for extracting an extracted clock signal out of a periodic data signal by means of a circuit according to one of the preceeding claims, comprising:

(a1) generating a rising edges clock signal,

(a2) detecting a first phase difference between a rising edge of the periodic data signal and a rising edge of a rising edges clock signal;

(a3) generating the rising edges clock signal in a way that the detected first phase difference is minimal by feeding back the rising edges clock signal to the first phase detector (104) via a first loop formed between a first output of the first clock generator (110) and a first input of the first phase detector (104),

(b1) generating a falling edges clock signal,

(b2) detecting a second phase difference between a falling edge of the periodic data signal and a falling edge of a falling edges clock signal;

(b3) generating the falling edges clock signal in a way that the detected second phase difference is minimal by feeding back the falling edges clock signal to the second phase detector (106) via a second loop formed between a second output of the second clock generator (112) and a second input of the second phase detector (106),

(c) generating the extracted clock signal based on an average of the first phase difference and the second phase difference in a way that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged.

New Claims

~~1. A clock signal extraction device for extracting a clock~~ signal from a periodic data signal, comprising:

- a phase detector (104, 106) for detecting a first phase difference between a rising edge of the data signal and a rising edges clock signal and for detecting a second phase difference between a falling edge of the data signal and a falling edges clock signal; and
- a clock generator (110, 112) for generating the rising edges clock signal, the falling edges clock signal and the clock signal
  - the clock generator (110, 112) comprising a first output connected to a first input of the first phase detector 104 forming a first loop, the clock generator (110, 112) and the first phase detector (104, 106) are coupled via the first loop and operate in a way that the detected first phase difference is minimal,
  - the clock generator (110, 112) comprising a second output connected to a second input of the second phase detector 106 forming a second loop, the clock generator (110, 112) and the second phase detector (104, 106) are coupled via the second loop and operate in a way that the detected second phase difference is minimal,
  - the clock generator (110, 112) generates the clock signal based on an average of the first phase difference and the second phase difference~~.~~

2. The device according to claim 1,
c h a r a c t e r i z e d i n t h a t
the clock generator comprises:

- a first clock generator (110) for generating the rising edges clock signal;

- a second clock generator (112) for generating the falling edges clock signal;
- a third clock generator (114) for generating the clock signal; and
- a controller (108) for processing the first phase difference and the second phase difference and for controlling the first, second and third clock generator (110, 112, 114).

3. The device according to claim 2, characterized in that the controller (108) being arranged between output terminals of the first and second phase detectors (104, 106) and respective input terminals of the first, second and third generators (110, 112, 114).

~~11. A method for extracting a clock signal from a periodic~~ data signal, comprising:

- detecting a first phase difference between a rising edge of the data signal and a rising edges clock signal and detecting a second phase difference between a falling edge of the data signal and a falling edges clock signal; and
- generating the rising edges clock signal so that the first phase difference is minimized, generating the falling edges clock signal so that the second phase difference is minimized, and generating the clock signal in dependence on the first phase difference and the second phase difference, the step of generating comprises generating the clock signal based on an average of the first phase difference and the second phase difference.
- generating the rising edges clock signal in a way that the detected first phase difference is minimal by feeding back the rising edges clock signal to the first phase detector

104via a first loop formed between a first output of the clock generator (110, 112) and a first input of the first phase detector 104,

- generating the falling edges clock signal in a way that the detected second phase difference is minimal by feeding back the falling edges clock signal to the second phase detector 104 via a second loop formed between a second output of the clock generator (110, 112) and a second input of the second phase detector 104,
- generating the clock signal based on an average of the first phase difference and the second phase difference.